

# Growth of Gold-assisted Gallium Arsenide Nanowires on Silicon Substrates via Molecular Beam Epitaxy

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## ABSTRACT

Gallium arsenide nanowires were grown on silicon (100) substrates by what is called the vapor-liquid-solid (VLS) growth mechanism using a molecular beam epitaxy (MBE) system. Good quality nanowires with surface density of approximately  $10^8$  nanowires per square centimeter were produced by utilizing gold nanoparticles, with density of  $10^{11}$  nanoparticles per square centimeter, as catalysts for nanowire growth. X-ray diffraction measurements, scanning electron microscopy, transmission electron microscopy and Raman spectroscopy revealed that the nanowires are epitaxially grown on the silicon substrates, are oriented along the [111] direction and have cubic zincblende structure.

## INTRODUCTION

Nanowires, or nanowiskers, are wire-like nanocrystals with diameters of several tens of nanometers and with length:diameter aspect ratios of 10 or more (Dubrovskii, et al., 2005). They are one-dimensional structures with unique growth mechanism and remarkable physical properties. One-dimensional systems such as nanowires and nanotubes are the smallest dimension structures that can be used for efficient transport of electrons and optical excitations. In some aspects semiconducting nanowires are complementary to carbon nanotubes, but in contrast to the latter they offer more flexibility with the choice of materials, which makes them more useful for various device architectures and functionalities. There is a growing interest in the synthesis and properties of semiconducting nanowires because established conventional semiconductor technologies such as junction formation, (Cui, et al., 2000, Gudiksen, et al., 2002) growth of heterostructures (Cui, et al., 2000, Gudiksen, et al. 2002) and doping can be potentially applicable to them.

## Current Trends in Nanowire Technology

At present, semiconducting nanowires are seen to be the most versatile building blocks for electrical, optical, and (opto) electronic circuits at the nanoscale. The use of semiconducting nanowires in electrical circuits ranges from transistor arrays, (Patolsky, et al., 2006) to single electron tunneling devices, (Franceschi et al. 2003) and nonvolatile memory (Duan, et al., 2002). They could also be used as electrical sensors (Patolsky, et al., 2006) due to their large surface-to-volume ratios that lead to higher sensitivity to changes at their surfaces or surroundings. A “bottom-up” approach to circuit assembly using nanowire building blocks (Huang, et al., 2006) can be useful for complementary opto-electrical functions. Some opto-electrical nanodevices based on semiconducting nanowires include polarization-dependent photo-detectors (Wang, et al., 2001), light emitting diodes (Gudiksen, et al., 2002) and solar cells (Law, et al., 2005). In addition, the nanowires can act as nanocavities for light resulting in optically- or electrically-driven nanolasers (Huang, et al., 2001, Duan, et al., 2003), and subwavelength waveguiding

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of light over long distances and through sharp bends (Barrelet, et al., 2004).

The compound semiconductor gallium arsenide (GaAs) is one of the most likely candidates as the choice for nanowire material because of its intrinsic direct bandgap which gives rise to attractive optical and optoelectrical properties, and also due to the already existing technological platform for this material. Particularly, epitaxial growth of GaAs nanowires on silicon (Si) substrates is of considerable importance because it can pave the way for the possible integration of high-performance III-V semiconductor nanoscale devices with well-established Si technology. This will likely happen since the growth of III-V compound semiconductor nanowires, such as GaAs nanowires, on Si can solve many problems associated with the large difference in lattice constant and structure (Martensson, et al., 2004).

### Vapor–liquid–solid (VLS) Growth Mechanism Overview

In general, the development of device-quality III-V semiconducting nanowires based on vapor–liquid–solid (VLS) reaction (Martensson, et al., 2004, Wagner & Ellis, 1964, Khorenko, et al., 2004) has the advantage over techniques such as photolithography, ion beam lithography, ion etching, and others because the lateral size of the nanoparticle metal-catalysts predefines the growth areas for the nanowires and controls the morphology of the as-grown nanostructures.

In the VLS growth mode, the metal nanoparticles are used to direct growth in a highly anisotropic or one-dimensional manner. This mechanism consists of three main stages which are illustrated in Figure 1A (Wagner & Ellis, 1964). First, a liquid eutectic alloy is produced from the nanoparticle and the growth elements. Next, the eutectic system absorbs more semiconductor material until a supersaturation condition is reached. When the supersaturated alloy droplet coexists with the solid phase of the semiconductor, nucleation occurs. Finally, a steady state is formed in which the semiconductor crystal grows at the solid/liquid interface. The precipitated semiconductor material grows as a wire because the growth area is limited by the area of the alloy droplet or the catalyst itself (Wagner & Ellis, 1964, Khorenko, et al., 2004). In the VLS mechanism, the nanowire diameter is determined by the diameter of the alloy particle that is formed from the metal nanoparticle and the growth elements; while the length is dependent on the growth rate, growth time and even on the lateral size of nanowires or Au seed particles (Dubrovskii, et al., 2005).

Examining the feasibility of the VLS wire growth for a certain compound semiconductor-metal system requires the study of the associated pseudo-binary phase diagram as illustrated in Figure 1B (Duan & Leiber, 2000). An isothermal line in the diagram will show the subsequent phases involved when a gold nanoparticle absorbs the semiconductor material at a constant temperature. The primary condition for VLS wire growth is that the metal should form an alloy with the

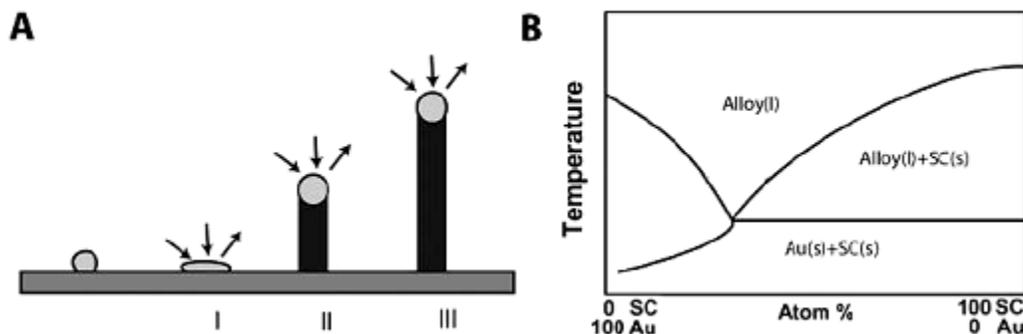


Figure 1. (A) The stages of: I) alloying, II) nucleation and III) development of nanowire synthesis, according to the VLS growth mechanism. (B) Pseudobinary phase diagram of a semiconductor-gold system.

semiconductor at a temperature that also allows the semiconductor to exist in the solid phase.

## MATERIALS AND METHODOLOGY

Samples used in this study were grown using the Riber 32P MBE facility at the National Institute of Physics, University of the Philippines Diliman. Prior to the growth itself, the Si (100) substrates were cleaned using the standard degreasing procedures and were subsequently immersed for 5 minutes in a diluted hydrofluoric acid to remove the native oxides. Right after the oxide removal, they were loaded inside an electron beam evaporator to deposit gold (Au) clusters (or islands) on their surfaces for various time intervals (i.e. 10 sec, 20 sec and 30sec), at a base pressure of  $8.8 \times 10^{-6}$  torr, using an emission current of 34 milliamperes. (The emission current of the electron beam dictates the rate at which the material is deposited on the substrates.) The gold-deposited Si substrates were then transferred into the  $N_2$ -ambient annealing tube furnace and were annealed at  $540^\circ\text{C}$  for 10 minutes to generate Au nanoparticles of diverse sizes and densities from the Au islands grown at different time intervals. Finally, they were all mounted onto a molybdenum substrate holder and were degassed inside the MBE growth chamber for 5 minutes at a temperature of  $585^\circ\text{C}$  under arsenic flux. GaAs nanowires on silicon substrates were grown at  $580^\circ\text{C}$  with an arsenic:gallium (As:Ga) flux ratio of 15 and a fixed Ga beam flux, which is required for the homoepitaxial GaAs growth rate of  $0.25\mu\text{m/hr}$  on a GaAs (100) substrate. The background pressure was  $10^{-9}$  torr during growth. The growth of GaAs nanowires

was ended by switching off the gallium supply while maintaining the arsenic supply until the substrate temperature cooled down to  $400^\circ\text{C}$  to stabilize the nanowires.

For the investigation of the crystalline quality and structural properties of the MBE-grown GaAs nanowires, scanning electron microscopy (SEM), transmission electron microscopy (TEM), Raman spectroscopy and X-Ray diffraction (XRD) analyses were performed. The samples for TEM were prepared by scratching a surface in order to separate the nanowires from the substrate and transfer them onto carbon-film-coated Cu grids.

## RESULTS AND DISCUSSION

### Electron Microscopy Characterization of Gold Nanoparticles

In this research, gold nanoparticles of different sizes and densities were utilized as catalysts for the VLS growth of nanowires. Surface morphology of the generated Au nanoparticles on silicon substrates was observed by acquiring SEM micrographs at different magnifications. Figures 2A up to 2C are images of Au nanoparticles on Si (100) substrates that were formed from the clusters deposited at different time intervals. Generally, the nanoparticles from the clusters grown for 30sec have the largest lateral size (approximately ranging from 10-30 nm) of the three sets, followed by the nanoparticles from the clusters grown for 20sec the diameters of which range from about 10-20 nm, while those that came from the clusters grown for 10sec

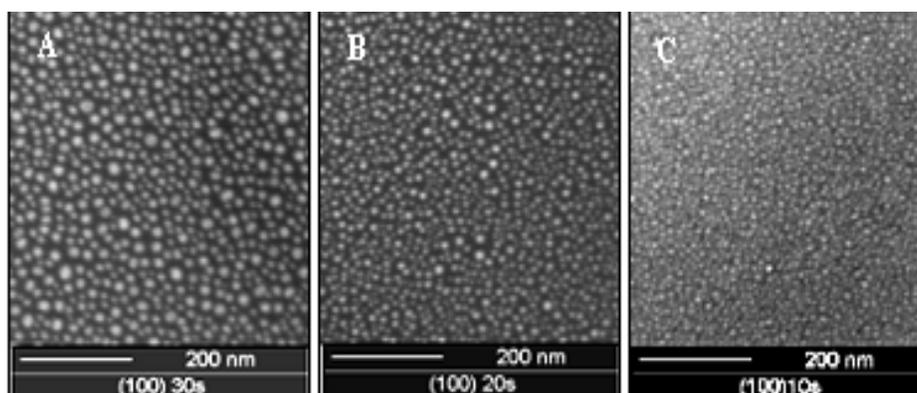
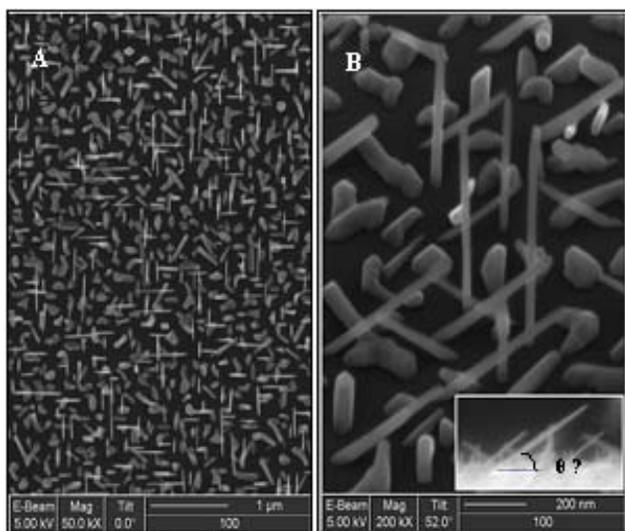


Figure 2A-C SEM micrographs of Au nanoparticles on Si (100) substrates generated from clusters deposited for: (A) 30 seconds; (B) 20 seconds; and (C) 10 seconds. All images were taken at a magnification of 200,000X.

are the smallest (roughly varying from 8-10 nm in diameter). The surface densities of Figures 2A, 2B and 2C are  $1.70 \times 10^{11}$ ,  $2.68 \times 10^{11}$  and  $3.38 \times 10^{11}$  nanoparticles per square centimeter, respectively. The differences in lateral sizes and surface densities among the three sets may be due to the fact that the density of the islands formed during the early stages of growth saturates quickly, and that the islands begin to grow in size by adsorbing atoms from the incident vapor beam and receiving atoms from the neighboring islands which eventually disappear (Maissel & Francombe, 1973, Bassett & Wenter & Pashley, 1959). Annealing the gold-deposited Si substrates at 540°C for 10 minutes improves the uniformity of the nanoparticles by enhancing the island agglomeration (Harmand, et al., 2007, Ihn, et al., 2006, Chan, et al., 2003, Hiruma, et al., 1995, Vosen, 1977).

### Electron Microscopy Characterization of Gallium Arsenide Nanowires

SEM micrographs of GaAs nanowires on Si (100) substrate with gold nanoparticles generated from clusters that were deposited for 10 seconds are given



**Figure 3A-B.** (A) Top view (with 50,000X magnification) and (B) 52°-tilted view (with 200,000X magnification), SEM images of GaAs nanowires grown at 580°C on gold-deposited Si (100) substrate. The inset in (B) is a cross-sectional image (with 45,000X magnification) of the same sample showing a nanowire inclined at approximately 35° from the substrate surface.

in Figures 3A and 3B. The images were acquired from one sample using three different magnifications and viewing angles. The GaAs nanowires were grown at 580°C for 15 minutes using a As:Ga flux ratio equal to 15 and a growth rate of 0.25  $\mu\text{m/hr}$ . The sample has a surface density of approximately  $9 \times 10^8$  GaAs nanowires per square centimeter. This value was obtained by considering a  $1 \mu\text{m} \times 1 \mu\text{m}$  area from the top view SEM image of the sample (Figure 3A) and counting the nanowires that can be found within that area.

Most of the nanowires of the sample were observed to be either parallel or perpendicular to one another, and at an angle of inclination roughly equal to 35° from the surface of the Si (100) substrate. This measured angle of inclination can also be calculated by looking at a cubic zincblende structure along the [111] axis (see Figure 4A) (Yu & Carolona, 1996). In this point of view, the computed value of the angle between the (111) and (100) planes is  $54.7^\circ$ , so that a nanowire that is assumed to be perpendicular to the (111) plane has an angle of inclination equal to 35.3 with respect to the (100) plane as shown in Figure 4B. Martensson et al. (2004) observed that on Si (100) substrate, GaP nanowires preferably grew in four equivalent  $\langle 111 \rangle$  directions which make an angle of  $35.3^\circ$  with the substrate surface, distributed  $90^\circ$  apart azimuthally as illustrated in Figure 5 (Martensson, et al., 2004). This is similar to what we have observed on the nanowire sample in Figure 3. Martensson et al. further argued that for epitaxial growth all four directions can be expected since the four  $\langle 111 \rangle$  directions are equivalent.<sup>14</sup> Epitaxial growth is characterized by an oriented layer by layer growth; this is illustrated by expressed parallelism of the deposited plane (and axis) and the plane (and axis) of the substrate (Maissel & Francombe, 1973). Thus, our results affirm that the synthesized GaAs nanowires on Si (100) substrate were the  $\langle 111 \rangle$  family in growth direction and they were epitaxially grown nanowires.

A TEM micrograph of the tip region of a single GaAs nanowire from a sample with gold nanoparticles generated from clusters that were deposited for 10 seconds is shown in Figure 6. This image was acquired to clearly resolve the lateral sizes of a representative GaAs nanowire and the Au nanoparticle on its tip which

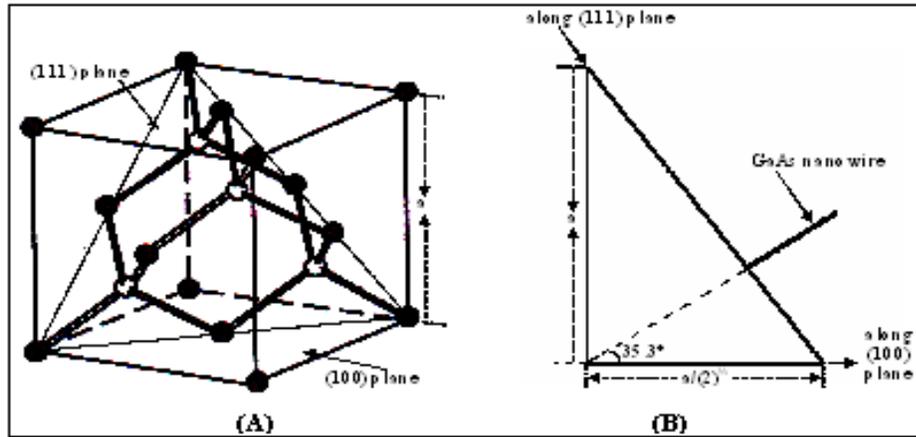


Figure 4A-B. (A) The crystal structure of a cubic zincblende. Note that if this figure is looked at along the [111] axis, we can visualize the orientation of the nanowires with respect to the (100) plane. (B) Diagram illustrating the angle 35.3°.

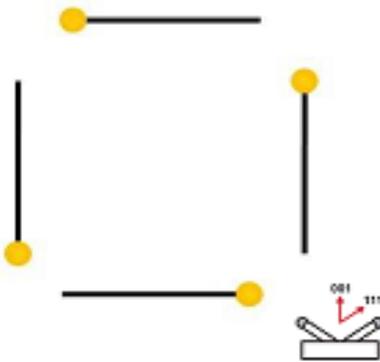


Figure 5. Azimuthal projections of four nanowires grown along the four equivalent  $\langle 111 \rangle$  directions on Si (100) substrate. The inset shows that the nanowires form an angle of 35.3° with the Si (100) surface.

cannot be done by employing SEM alone. The lateral size of the nanoparticle was measured to be approximately 12.6 nm and the average diameter of the nanowire to be 24.7 nm. That the nanowire was grown via the VLS growth method can be inferred from the very presence of the gold nanoparticle at the tip of the GaAs nanowire, since this is a characteristic feature of such a mechanism. The electron diffraction pattern from the TEM suggests that the majority of this region of the nanowire has cubic (zincblende) structure. This type of crystal structure is also the characteristic feature of bulk GaAs.

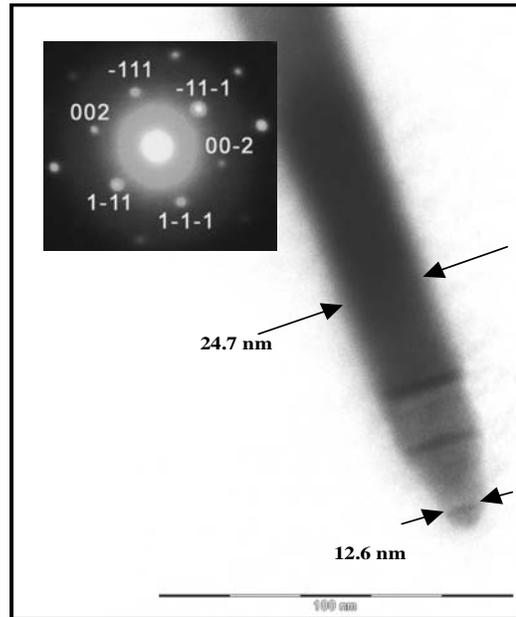


Figure 6. TEM image of the tip region of a single GaAs nanowire. The image was taken at a magnification of 500,000X. The scale bar is 100 nm long.

### XRD Analysis and Raman Spectroscopy Characterizations of Sample with GaAs Nanowires

The gold-assisted GaAs nanowires were also characterized by XRD analysis and Raman spectroscopy at room temperature. The result of theta/ two theta XRD scan from a sample with GaAs nanowires on Si (100) is shown in Figure 7 The normalized peaks are located at  $2\theta = 66.219^\circ, 69.118^\circ$

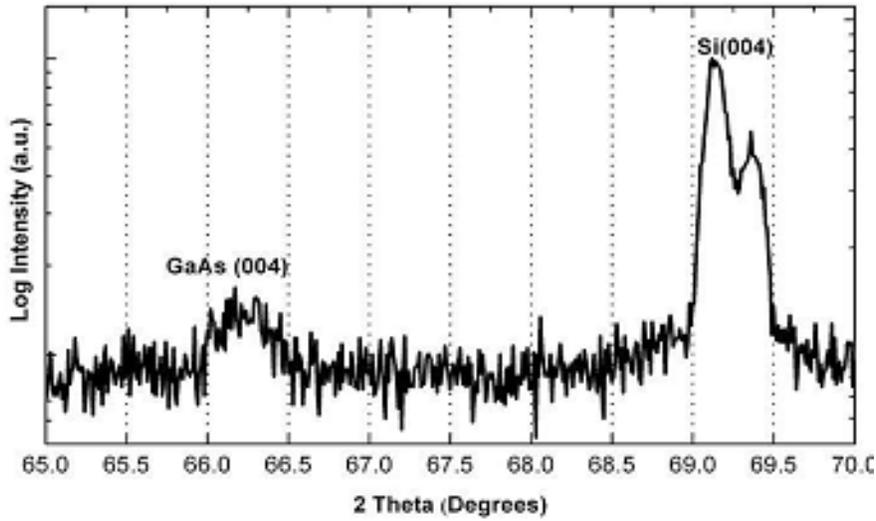


Figure 7. X-ray diffraction 2 scan from a sample with GaAs nanowires on Si (100) substrate.

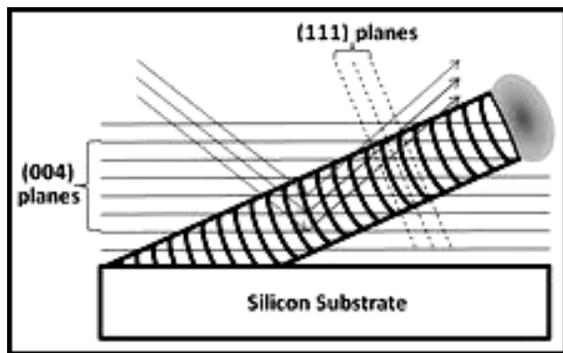


Figure 8. Diagram illustrating the {004} family of planes on a nanowire grown on Si (100) substrate. The angle between the wire and the substrate surface is 35.3°.

and 69.358°. The peak at  $2\theta = 66.219^\circ$  corresponds to the cubic zincblende GaAs (004) plane as confirmed by the Bragg's Law. Those at  $2\theta = 69.118^\circ$  and  $69.358^\circ$  are initially the characteristic peaks of a bare Si (100) substrate and are related to the (004) plane of the silicon material. Only one GaAs peak pertaining to the (004) plane was observed because the {004} family of planes on the nanowires were the ones directly exposed to the x-rays as illustrated in Figure 8.

A reference sample with very thin GaAs layer on bare (without gold nanoparticles) Si (100) substrate was also grown side by side with the nanowire sample to ensure similar growth conditions. The presence of a weak GaAs peak on the scan of the sample with GaAs nanowires, and its absence from that of the reference

sample with a thin layer of GaAs proves that the GaAs peak came from these nanostructures and that they exhibit good crystallinity. Due to the nanometer-sized diameters and large surface-to-volume ratios of the nanowires, the GaAs peak is expected to be broad. The core of a nanowire, which makes up the majority of the nanostructure, is expected to have true crystal lattice while those located near or at the surface have distorted lattice, and these contribute to the broadening of the peak. Also, according to Duan et al. (Duan, et al., 2000), a thin amorphous coat at the nanowire exterior is formed when GaAs nanowires are exposed to air;

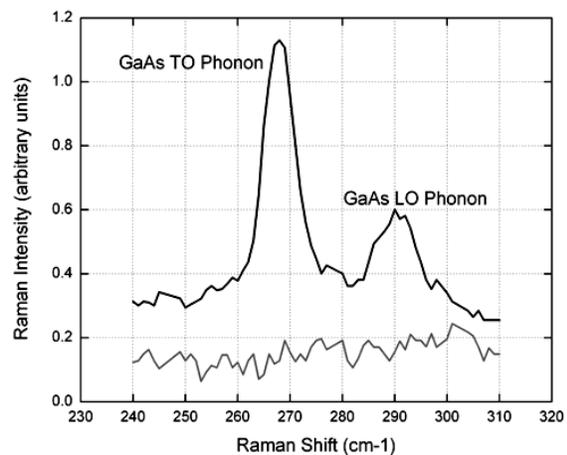


Figure 9. Raman spectra from (top) a sample with GaAs nanowires on Si (100) substrate; and (bottom) a gold-deposited Si (100) substrate. For the former sample, the Raman signals of the GaAs LO and TO phonons were observed at 292  $\text{cm}^{-1}$  and 268  $\text{cm}^{-1}$ , respectively.

this amorphous coat causes the broadening of the GaAs diffraction peak.

Normalized Raman spectrum from a sample with GaAs nanowires on Si (100) substrate, together with a reference spectrum obtained from a gold-deposited Si (100) substrate are shown in Figure 9. The Raman shift (in terms of wavenumbers) scan range was intentionally restricted to examine only the vibrational modes for GaAs material and exclude those associated with Si and even Au. For the sample with GaAs nanowires, the Raman signals of the GaAs longitudinal optical (LO) and transverse optical (TO) phonons were observed at  $292\text{ cm}^{-1}$  and  $268\text{ cm}^{-1}$ , respectively. For bulk GaAs, the signal for LO phonon is at  $290.2\text{ cm}^{-1}$ , while the signal for TO phonons is located at around  $268.6\text{ cm}^{-1}$ . Moreover, the peak of LO phonon for bulk GaAs has a higher intensity than that of the TO phonon (Mahan, et al., 2003). According to the results, and as seen on the graph, the GaAs TO phonon signal is much stronger than that related to the GaAs LO phonon, as also previously observed by Begum et al. (Begum, et al., 2008). The full width at half maximum (FWHM) of the LO phonon signal is equal to eight wavenumbers, while the one associated with the TO phonon signal is about seven wavenumbers. The existence of these two prominent Raman signals associated with the GaAs nanowires indicates the good crystal quality of the GaAs material. At present, further investigations on the nature of the relative intensities of the Raman peaks are still being carried out.

### Summary of Results

Good quality GaAs nanowires epitaxially grown on Si (100) substrates by using Au-catalyzed VLS growth with an MBE system were demonstrated. The sample with nanowires was found to have a surface density of approximately  $9 \times 10^8$  GaAs nanowires per square centimeter. The synthesized nanowires on Si (100) substrate were epitaxially grown along the [111] direction and they have cubic (zincblende) crystal structure. TEM imagery showed that the average diameter of a representative nanowire from the sample with Au nanoparticles generated from clusters that were deposited for 10 seconds is 24.7 nm. From the results of the XRD measurements, the presence of a GaAs peak at  $2\theta = 66.219^\circ$  for a sample with GaAs

nanowires and its absence for a sample with only a thin layer of GaAs on bare Si (100) proves that the GaAs peak came from these nanostructures and that they exhibit good crystallinity. Lastly, the Raman signals of the GaAs longitudinal optical (LO) phonon observed at  $292\text{ cm}^{-1}$  and GaAs transverse optical (TO) phonon at  $268\text{ cm}^{-1}$  from a sample with GaAs nanowires indicate the good crystal quality of the GaAs material.

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